A 7-decades Tunable Translinear SiGe BiCMOS 3-phase Sinusoidal Oscillator

Dimitrios N. Loizos[1,2], Paul P. Sotiriadis[2] and Gert Cauwenberghs[1]

[1]Division of Biological Sciences, University of California, San Diego, CA 92093
[2]Department of Electrical and Computer Engineering, The Johns Hopkins University, Baltimore, MD 21218

***Abstract*— A fully differential translinear 3-phase sinusoidal oscillator architecture is presented. The architecture is meant for BiCMOS implementation and uses only NPN devices, typically of higher performance than their PNP counterparts in most technologies. The architecture features both frequency and amplitude control and expressions are derived showing the dependence of these controls to external current biases. Measurements on a 0.5μm SiGe BiCMOS implementation of the architecture demonstrate frequency control from below 80Hz to above 800MHz, general agreement between theory and actual data for the amplitude of oscillation, as well as low distortion. Power consumption scales with the frequency of operation and amounts to ∼2μW/MHz.**

I. Introduction

Wide range frequency synthesis finds a fertile ground in many applications. Combining wide range oscillators in PLLs, multi-decade spurious-free frequency synthesis can be accomplished by appropriately mixing the outputs from multiple fractional-N synthesizers [1]. Oscillators covering a broad range of frequencies can be useful for built-in self test of analog and mixed-signal integrated circuits [2], [3]. Incorporation of wide range oscillators in synchronous detection schemes for characterizing and controlling linear and nonlinear systems has been demonstrated [4]. Applications in biology have been also reported, such as e.g. in generating rotating electrical fields in studies of the ac electrokinetics of biological cells [5], [6].

The inadequacy of LC-tuned or crystal-based oscillator networks for the generation of wide-range tunable oscillations has led to several designs using only resistors, capacitors and amplifiers. Although MOSFET based oscillators have been reported [7], [8] with significantly wide ranges and maximum attainable frequencies, it has been mainly with translinear designs based in bipolar transistor architectures, that tuning ranges of 5 or more decades, spanning frequencies up to tens or hundreds of MHz, have been achieved using a single control signal. Exploiting the validity of the linear relation between transconductance and biasing current in bipolar transistors over an extremely wide range, $G_m - C$ based [9], log-domain filter based [10] and current-conveyor based [11] translinear oscillators have been presented. In [12] a quadrature oscillator spanning 6 decades of frequency tuning has been implemented using a dynamic translinear (log-domain) method.

Purpose of the work presented here is to propose a translinear design of a 3-phase oscillator, able to generate frequencies over a wide range by means of a single control. A 3-phase version has been chosen since the oscillator is meant for phase-compensated synchronous detection, where the need of multiple phases is apparent. The main difference compared to previously reported designs is the use of only NPN bipolar transistors in the architecture, thus avoiding PNP devices of generally inferior performance in typical BiCMOS technologies, and allowing for high frequency oscillations. A fully differential design has been implemented in order to minimize distortion, and amplitude control through an external biasing current has been added. Section II describes the general proposed architecture while Section III introduces the actual circuit implementation. In Section IV expressions for the amplitude and frequency of oscillation are derived and in Section V experimental results are discussed.

II. Architecture

A block diagram of the proposed 3-phase oscillator is shown in Fig. 1. It consists of 3 identical modules acting as 1st order low-pass filters, each having a gain of 1 and inserting a phase shift of 60° in the loop at the frequency of oscillation. The additional 180° needed for oscillations are provided by signal inversion at the output of each module.

For the sake of simplicity, the ideal case of linear gain stages is first considered, as cascades of a linear transconductance G_m and a linear resistor R, as shown in Fig. 2. Each $G_m - R - C$ module will exhibit a gain of

$$|H(j\omega)| = \frac{G_m R}{\sqrt{1+(\omega RC)^2}}$$

and contribute to the loop a phase of

$$\tan^{-1}\left(H(j\omega)\right) = -\omega RC.$$

Applying the Barkhausen oscillation criterion (gain around the loop is 1 and the total phase equals $k{\cdot}360°$, k being an integer),

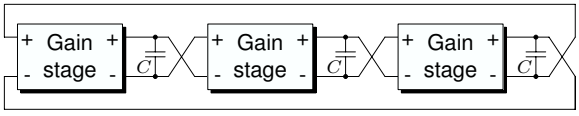

Fig. 1. Block diagram architecture of the proposed 3-phase oscillator. Cross-coupled 1st order low-pass filters provide a total phase of 360° at the frequency of oscillation.

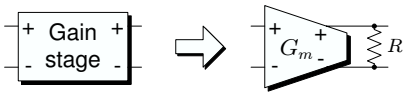

Fig. 2. Implementation of a linear gain stage using a cascade of a linear transconductor G_m and a linear resistor R.

the following conditions for oscillation are derived

$$R = \frac{2}{G_m} \tag{1}$$

$$\omega = \frac{\sqrt{3}G_m}{2C}. \tag{2}$$

According to (2), the frequency of oscillation ω is linearly controlled by transconductance G_m. Appealing from a circuits point of view is the use of translinear networks for the implementation of the architecture. Taking advantage of the linear dependence between transconductance and biasing current in such networks over a wide range, the oscillation frequency can be tuned over multiple decades through a single parameter, as will be shown in the following Section.

Equation (1) points the need of having the load R following any changes in the transconductance G_m. Therefore, R has also to be tunable and scale inversely proportionally to G_m.

III. Circuit implementation

A possible circuit design for the $G_m - R$ block is shown in Fig. 3. Transconductance G_m (transistors Q_1 and Q_2) and resistance R (diodes $D_1 - D_6$) have been combined into a translinear network and are both controlled by the same bias current, thus linking any changes of G_m to R. All transistors in the network are equally sized and the total DC gain is $A = G_m \cdot R = 3$. Since A is higher than the gain required for oscillations according to (1), the amplitude of the state variables u and v is expected to grow until any of the transistors start to enter the cut-off region. Transconductance G_m and, through (2), the frequency of oscillation are linearly controlled by I_F.

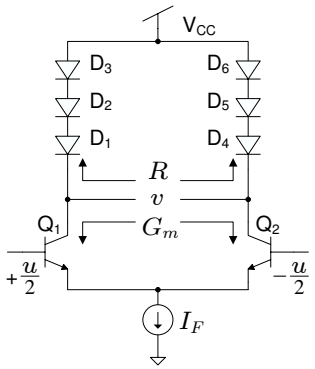

Fig. 3. Possible circuit implementation of the $G_m - R$ module. The architecture is fully translinear and avoids PNP devices, however requires a large voltage headroom.

A downfall to the previous design is the need for excessive voltage headroom, usually not available in typical BiCMOS processes. In order to comply with the 3.3V requirement for the power supply in most BiCMOS technologies, the design of Fig. 4 is proposed for the implementation of the $G_m - R$ blocks in the oscillator architecture. Current sources I_A have been included for amplitude control, as will be shown next.

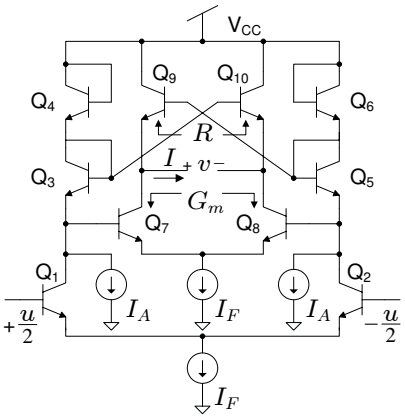

Fig. 4. Proposed translinear implementation of the $G_m - R$ module.

IV. Circuit analysis

A. Circuit operation

Denoting as u the differential input voltage to the network of Fig. 4 and as v its differential output, analysis of the circuit reveals that the input-output relation of the translinear amplifier will be

$$v = 3V_T \ln\left(\frac{e^{\frac{u}{V_T}} + \beta\left(1 + e^{\frac{u}{V_T}}\right)}{1 + \beta(1 + e^{\frac{u}{V_T}})}\right) \tag{3}$$

where $V_T = \frac{kT}{q}$ is the thermal voltage, typically 25mV, and $\beta = \frac{I_A}{I_F}$. Setting $I_A = 0$A, equation (3) collapses to $v = 3u$, providing, as in the case of Fig. 3, a translinear network of DC gain $A = 3$. Transition of the transistors into the cut-off region will be again the factor limiting the amplitude of oscillation.

For $\beta > 0$, the input-output voltage relation is no longer linear, and as long as the transistors do not enter their cut-off region, the amplitude will be limited by the nonlinearities of the circuit. Current I_A provides the flexibility of controlling the shape of the input-output curve and therefore can be used as a tuning parameter for the amplitude.

The translinear network exhibits maximum gain $A_{\max}$ for 0 input and the gain is derived by evaluating the derivative of v with respect to u (equation (3)) for $u = 0$. $A_{\max}$ can be also viewed as the small signal gain of the translinear circuit around the origin $(u, v) = (0, 0)$ and compared to condition (1) that has been derived for the linear network of Fig. 2. For oscillations to start $A_{\max} > 2$ is needed, which gives an upper limit for β

$$0 \leq \beta < 0.25 \Leftrightarrow 0 \leq I_A < 0.25 I_F \tag{4}$$

B. Frequency

In order to derive the frequency of oscillation, first the output current charging capacitor C of the translinear $G_m - R-C$ block is expressed as a function of the input and output voltages u and v. Analysis of the circuit leads to the following relation

$$I = f(u,v) = \frac{I_F\left(k^3(u) - e^{\frac{v}{V_T}}\ell^3(u)\right)}{\left(k^2(u)+\ell^2(u)\right)\left(k(u)+e^{\frac{v}{V_T}}\ell(u)\right)} \quad (5)$$

where

$$k(u) = e^{\frac{u}{V_T}} + \beta\left(1+e^{\frac{u}{V_T}}\right)$$
$$\text{and} \quad \ell(u) = 1+\beta\left(1+e^{\frac{u}{V_T}}\right)$$

Assuming smooth non-linearity of the expression $I = f(u,v)$ at the region of operation, function f can be approximated by its Taylor expansion including terms up to 3rd order. Noting the symmetry of the circuit and its differential nature, even order terms will be 0 and f can be written as

$$f(u,v) \simeq a_1u + a_2v + b_1u^3 + b_2u^2v + b_3uv^2 + b_4v^3 \quad (6)$$

The Taylor expansion coefficients a and b can be evaluated by appropriate scaling of the partial derivatives of f with respect to u and v.

Next, expression (6) is substituted to the state equations of the oscillatory system, that can be represented for each node as

$$C\dot{v} = f(u,v) \quad (7)$$

Under the assumption that each $G_m - R - C$ block filters higher order harmonics preserving only the fundamental, and taking into account the 60° phase shift that each block introduces, the input u and output v can be written as

$$u = A\cdot\sin(\omega t)$$
$$v = A\cdot\sin(\omega t - \tfrac{\pi}{3}) \quad (8)$$

where A is the amplitude of oscillation.

Combining (6), (7) and (8), the frequency of oscillation ω is derived

$$\omega = \frac{\sqrt{3}}{2}\cdot\frac{I_F}{V_TC}\cdot\frac{3+4\beta+2\beta^2}{7+6\beta-16\beta^3}. \quad (9)$$

C. Amplitude

A different approach has been followed in order to calculate the amplitude of oscillation, yielding an expression that describes better the operation of the circuit, as will be shown in the next Section. Starting from (3), the voltage gain of the translinear amplifier of Fig. 4 is derived by taking the derivative of the output voltage v with respect to the input u

$$\frac{dv}{du} = 3\frac{1+2\beta}{\left(1+\beta\left(1+e^{-u}\right)\right)\left(1+\beta\left(1+e^{u}\right)\right)}. \quad (10)$$

According to the linear version of the oscillator discussed in Section II and (1), this gain needs to equal 2 for oscillations to be sustained. Since the gain is input dependent in the nonlinear version, the linear criterion (1) is extended and assumed to hold also for the time averaged value of the gain of the nonlinear translinear amplifier. Linearizing (10) in the form of a Taylor series with terms up to 5th order and assuming oscillations at frequency ω and of amplitude A, the following requirement

$$\frac{1}{2\pi}\int_0^{2\pi}\left.\frac{dv}{du}\right|_{u=A\sin(\theta)} d\theta = 2,\ \theta=\omega t$$

leads to the expression of equation (11), at the bottom of the page, for the amplitude of oscillation.

V. Experimental results

The oscillator was fabricated in an IBM SiGe BiCMOS process provided through MOSIS with a resolution of 0.5μm and an f_T for the NPN devices of 50GHz. The chosen capacitor values were 0.5pF and the supply voltage was set at 3.3V. Power consumption scaled according to the frequency of operation and was close to 2μW/MHz. A microphotograph of the oscillator is shown in Fig. 5.

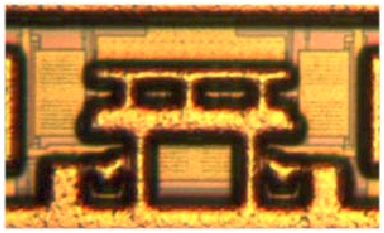

Fig. 5. Chip microphotograph of the oscillator. Dimensions are approximately 150μm×300μm in 0.5μm BiCMOS SiGe technology.

A first set of experiments was performed in order to derive the relation between current I_F and the frequency of oscillations. The results are shown in Fig. 6, demonstrating a linear frequency tuning range of 5 decades. The total range of achievable oscillations extends over 7 decades, from below 80Hz to above 800MHz. For the measurements, β was set to 0 in order to generate oscillations of maximum amplitude.

Figure 7 compares the theoretical expression (11) with measured results on the dependence of the amplitude to the ratio β. I_F is kept constant and β is controlled by current I_A,

$$A = 8\left(1+2\beta\right)\frac{\sqrt{3\beta\left(-1+7\beta+16\beta^2+8\beta^3\right)\left(6\beta^2+6\beta-\sqrt{372\beta^4+144\beta^3-30\beta^2+6\beta+192\beta^5}\right)}}{-12\beta+84\beta^2+192\beta^3+96\beta^4} \quad (11)$$

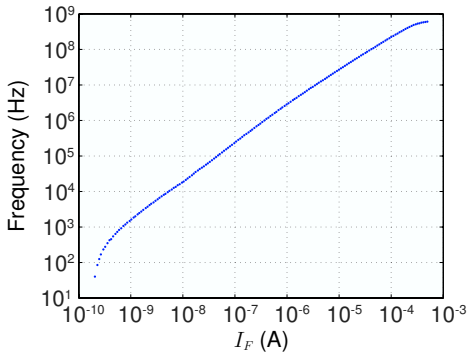

Fig. 6. Dependence of the oscillation frequency to current I_F. The range of measured frequencies spans 7 decades.

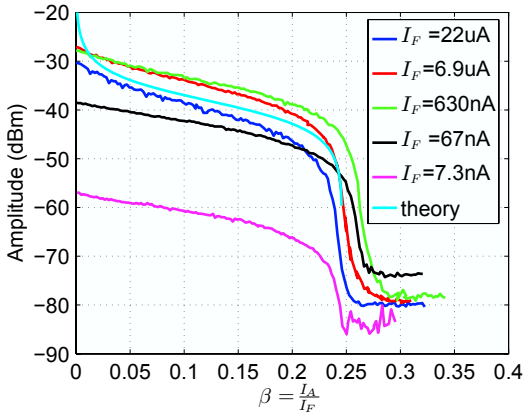

Fig. 7. Dependence of the amplitude of oscillation to β for several fixed values of I_F.

that was appropriately scaled to correct systematic errors in the current mirror ratios. For low currents I_F the amplitude of oscillation drops significantly. This is due to the reduced value of the forward current gain (β_F) of the transistors at low biasing currents, causing the translinear analysis to no longer hold and the oscillator to no longer operate as expected.

Finally, the spectrum of the output signal from one of the phases of the oscillator is plotted in Fig. 8, for a set frequency of 100MHz. Note that although the architecture is fully differential, measurements have been taken from only one of the outputs, justifying the presence of a second harmonic. The differential output will have only a third (and higher order odd) harmonic(s), which according to Fig. 8 is more than 40dB below the fundamental. Its low distortion makes this oscillator architecture a possible candidate for communication systems that require pure sinusoidal signals.

VI. Conclusion

A BiCMOS architecture of a 3-phase sinusoidal oscillator with amplitude and frequency control has been presented. The architecture is fully differential, uses only NPN devices and takes advantage of the linearity over a wide range between transconductance and biasing current in translinear networks. Expressions for the amplitude and frequency of oscillation as

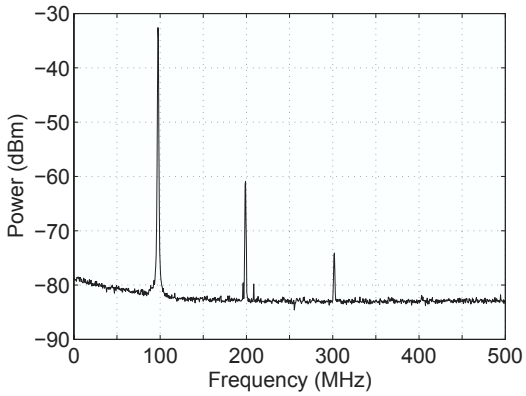

Fig. 8. Spectrum of the output signal from one of the phases of the oscillator for a generated frequency of 100MHz. The presence of the second harmonic is due to the single output measurement. In the actual differential output, the second harmonic is absent.

functions of externally controlled biasing currents have been derived. A SiGe BiCMOS implementation has been tested and the results demonstrate frequency control over 7 decades as well as low distortion. Amplitude data show a general trend similar to that predicted by theory.

VII. Acknowledgments

The authors would like to acknowledge the MOSIS Educational Program for providing the fabrication of the chip.

References

[1] P. P. Sotiriadis, "Diophantine frequency synthesis," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 53, no. 11, pp. 1988–1998, nov 2006.

[2] G. W. Roberts and A. K. Lu, *Analog Signal Generation for Built-in-Self-Test of Mixed-Signal Integrated Circuits*. Springer, 1995.

[3] M. Burns and G. W. Roberts, *An Introduction to Mixed-Signal IC Test and Measurement*. Oxford University Press, 2000.

[4] D. N. Loizos, P. P. Sotiriadis, and G. Cauwenberghs, "A robust continuous-time multi-dithering technique for laser communications using adaptive optics," in *Proc. Int. Symp. Circuits and Systems (ISCAS '06)*, May 2006, pp. 3626–3629.

[5] R. Hölzel, "A simple wide-band sine wave quadrature oscillator," *IEEE Trans. Instrum. Meas.*, vol. 42, no. 3, pp. 758–760, jun 1993.

[6] Y. Huang, R. Hölzel, R. Pethig, and X.-B. Wang, "Differences in the AC electrodynamics of viable and non-viable yeast cells determined through combined dielectrophoresis and electrorotation studies," *Phys. Med. Biol.*, vol. 37, no. 7, pp. 1499–1517, 1992.

[7] M. Banu, "MOS oscillators with multi-decade tuning range and gigahertz maximum speed," *IEEE J. Solid-State Circuits*, vol. 23, no. 6, pp. 1386–1393, dec 1988.

[8] T. Serrano-Gotarredona and B. Linares-Barranco, "7-decade tuning range CMOS OTA-C sinusoidal VCO," *Electron. Lett.*, vol. 34, no. 17, pp. 1621–1622, Aug. 20, 1998.

[9] B. Gilbert, "Current controlled quadrature oscillator based on differential G_M/C cells," 1996, U.S. Patent 5,489,878.

[10] S. Pookaiyaudom and J. Mahattanakul, "A 3.3 Volt high-frequency capacitorless electronically-tunable log-domain oscillator," in *Proc. Int. Symp. Circuits and Systems (ISCAS '95)*, May 1995, pp. 829–832.

[11] W. Kiranon, J. Kesorn, and P. Wardkein, "Current controlled oscillator based on translinear conveyors," *Electr. Lett.*, vol. 32, no. 15, pp. 1330–1331, Jul. 1996.

[12] W. A. Serdijn, J. Mulder, A. C. van der Woerd, and A. H. M. van Roermund, "A wide-tunable translinear second-order oscillator," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 195–201, Feb. 1998.